

ABSTRACT

An apparatus and method that utilizes partial ordering of ternary hierarchical addresses and their associated masks entries in both binary and ternary content addressable memories (CAMs) for providing fast searches and while reducing address
5 table size used in the processing of communication system (e.g., Internet Protocol (IP), layer-3 switches and ATM switches using E.164 addressing) addresses for identifying the source and destination of each digital packet data.